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Design and Assembly Process Implementation for BGAs

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Users of this publication are encouraged to participate in the development of future revisions.

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Table of Contents

1 SCOPE 1
1.1 Purpose 1
1.2 Selection Criteria (Determination of Package Style and Assembly Processes) 1
1.2.1 Technology Comparison 4

2 APPLICABLE DOCUMENTS 7
2.1 IPC 7
2.2 JEDEC 7

3 MANAGING BGA IMPLEMENTATION 7
3.1 Description of Infrastructure 8
3.1.1 Land Patterns and Circuit Board Considerations 8
3.1.2 Assembly Equipment Impact 8
3.1.3 Stencil Requirements 8
3.1.4 Inspection Requirements 8
3.1.5 Test 8
3.2 Time to Market Readiness 9
3.3 Methodology 9
3.4 Process Step Analysis 9
3.5 BGA Limitations and Issues 9
3.5.1 Visual Inspection 9
3.5.2 Moisture Sensitivity 9
3.5.3 Thermally Unbalanced BGA Design 10
3.5.4 Rework 10
3.5.5 Cost 10
3.5.6 Availability 10
3.5.7 Voids in BGA 10
3.5.8 Standardization Issues 11
3.5.9 Reliability Concerns 12

4 COMPONENT CONSIDERATIONS 12
4.1 Component Packaging Comparisons and Drivers 12
4.1.1 Package Feature Comparisons 12
4.1.2 BGA Package Drivers 12
4.1.3 Cost Issues 12
4.1.4 Component Handling 12
4.1.5 Thermal Performance 13
4.1.6 Real Estate 13
4.1.7 Electrical Performance 13
4.2 Die Mounting in the BGA Package 13
4.2.1 Wire Bond 13
4.2.2 Flip Chip 14
4.3 Standardization 15
4.3.1 Industry Standards for BGA 15
4.3.2 Ball Pitch 16
4.3.3 BGA Package Outline 17
4.3.4 Ball Size Relationships 17
4.3.5 Coplanarity 17
4.4 Component Packaging Style Considerations 18
4.4.1 Solder Ball Contact Alloy 18
4.4.2 Ball Attach Process 18
4.4.3 Ceramic Ball Grid Array 19
4.4.4 Ceramic Column Grid Arrays 19
4.4.5 Tape Ball Grid Arrays 20
4.4.6 Multiple Die Packaging 20
4.4.7 3D Folded Package Technology 21
4.4.8 Ball Stack Packaging 21
4.4.9 Folded and Stacked Packaging 21
4.4.10 Benefits of Multiple Die Packaging 22
4.5 BGA Connectors 22
4.5.1 Assembly Considerations for BGA Connectors 22
4.5.2 Material Considerations for BGA Connectors 22
4.6 BGA Construction Materials 23
4.6.1 Types of Substrate Materials 23
4.6.2 Properties of Substrate Materials 24
4.7 BGA Package Design Considerations 24
4.7.1 Power and Ground Planes 24
4.7.2 Signal Integrity 25
4.7.3 Heat Spreader Incorporation Inside the Package 25
4.8 BGA Package Acceptance Criteria and Shipping Format 25
4.8.1 Missing Balls 25
4.8.2 Voids in Solder Balls 25
4.8.3 Solder Ball Attach Integrity 26
4.8.4 Package Coplanarity 26
4.8.5 Moisture Sensitivity (Baking, Storage, Handling, Rebaking) 27
4.8.6 Shipping Medium (Tape and Reel, Trays, Tubes) 27

5 PCBS AND OTHER MOUNTING STRUCTURES . 28
5.1 Types of Mounting Structures 28
5.1.1 Organic Resin Systems 28
5.1.2 Inorganic Structures 28

5.1.3 Layering (Multilayer, Sequential or Build-Up) 28
5.2 Properties of Mounting Structures 29
5.2.1 Resin Systems 29
5.2.2 Reinforcements 29
5.2.3 Thermal Expansion 29
5.2.4 Glass Transition Temperature 30
5.2.5 Moisture Absorption 30
5.3 Surface Finishes 30
5.3.1 Hot Air Solder Leveling 30
5.3.2 Organic Surface Protection 31
5.3.3 Noble Platings/Coatings 32
5.4 Solder Mask 34
5.4.1 Wet Vs. Dry Film Solder Masks 34
5.4.2 Photoimageable Solder Masks 35
5.4.3 Registration 35
5.4.4 Via Filling 35
5.5 Thermal Structure Incorporation (e.g., Metal Core Boards) 37
5.5.1 Lamination Sequences 39
5.5.2 Heat Transfer Pathway 39

6 PRINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATION 39
6.1 Component Placement and Clearances 39
6.1.1 Pick and Place Requirements 39
6.1.2 Repair/Rework Requirements 39
6.1.3 Global Placement 40
6.1.4 Alignment Legends (Silkscreen, Copper Features, Pin 1 Identifier) 40
6.2 Attachment Sites (Land Patterns and Vias) 40
6.2.1 Big Vs. Small Land and Impact on Routing 40
6.2.2 Solder Mask Vs. Metal Defined Land Design . 41
6.2.3 Conductor Width 42
6.2.4 Via Size and Location 42
6.3 Escape and Conductor Routing Strategies 43
6.3.1 Uncapped Via-in-Pad and Impact on Reliability Issue 44
6.4 Impact of Wave Solder on Top Side BGAs 45
6.4.1 Top Side Reflow 45
6.4.2 Impact of Top Side Reflow 46
6.4.3 Methods of Avoiding Top Side Reflow 46
6.4.4 Top Side Reflow for Lead Free Boards 48
6.5 Testability and Test Point Access 48
6.5.1 Component Testing 48
6.5.2 Damage to the Solder Balls During Test and Burn-In 48
6.5.3 Bare Board Testing 49
6.5.4 Assembly Testing 51
6.6 Other Design for Manufacturability Issues 52
6.6.1 Panel/Subpanel Design 52
6.6.2 In-Process/End Product Test Coupons 52
6.7 Thermal Management 53
6.7.1 Conduction 54
6.7.2 Radiation 54
6.7.3 Convection 54
6.7.4 Thermal Interface Materials 54
6.7.5 Heat Sink Attachment Methods for BGAs 56
6.8 Documentation 57
6.8.1 Drawing Requirements 57
6.8.2 Electronic Data Transfer 58
6.8.3 Specifications 58

7 ASSEMBLY OF BGAS ON PRINTED CIRCUIT BOARDS 58
7.1 SMT Assembly Processes 58
7.1.1 Solder Paste and Its Application 58
7.1.2 Component Placement Impact 59
7.1.3 Vision Systems for Placement 59
7.1.4 Reflow Soldering and Profiling 60
7.1.5 Cleaning Vs. No-Clean 62
7.1.6 Package Standoff 63
7.1.7 Equipment Messaging Protocols 63
7.2 Post-SMT Processes 65
7.2.1 Conformal Coatings 65
7.2.2 Depaneling of Boards and Modules 65
7.3 Inspection Techniques 66
7.3.1 X-Ray Usage 66
7.3.2 X-Ray Image Acquisition 68
7.3.3 Definition and Discussion of X-Ray System Terminology 68
7.3.4 Analysis of the X-Ray Image 71
7.3.5 Scanning Acoustic Microscopy 72
7.3.6 BGA Standoff Measurement 72
7.3.7 Optical Inspection 73
7.3.8 Destructive Analysis Methods 74
7.4 Testing and Product Verification 75
7.4.1 Electrical Testing 75
7.4.2 Test Coverage 75
7.4.3 Burn-In Testing 76
7.4.4 Accelerated Testing 76
7.4.5 Product Screening Tests 76
7.5 Assembly Process Control Criteria for Plastic BGAs 76
7.5.1 Voids 76

7.5.2 Solder Bridging 83
7.5.3 Opens 84
7.5.4 Cold Solder 84
7.5.5 Defect Correlation/Process Improvement 84
7.5.6 Insufficient/Uneven Heating 84
7.5.7 Component Defects 84
7.6 Repair Processes 85
7.6.1 Rework/Repair Philosophy 85
7.6.2 Removal of BGA 85
7.6.3 Replacement 86

8 RELIABILITY 88
8.1 Damage Mechanisms and Failure of Solder Attachments 88
8.2 Solder Joints and Attachment Types 88
8.2.1 Global Expansion Mismatch 88
8.2.2 Local Expansion Mismatch 89
8.2.3 Internal Expansion Mismatch 89
8.3 Solder Attachment Failure 89
8.3.1 Solder Attachment Failure Classification 89
8.3.2 Failure Signature-1: Cold Solder 89
8.3.3 Failure Signature-2: Land, Nonsolderable 89
8.3.4 Failure Signature-3: Ball Drop 90
8.3.5 Failure Signature-4: Missing Ball 90
8.3.6 Failure Signature-5: Package Warpage 90
8.3.7 Failure Signature-6: Mechanical Failure 90
8.3.8 Failure Signature-7: Insufficient Reflow 91
8.4 Critical Factors to Impact Reliability 91
8.4.1 Package Technology 91
8.4.2 Standoff Height 92
8.4.3 PCB Design Considerations 92
8.4.4 Reliability of Solder Attachments of Ceramic Grid 93
8.4.5 Lead Free Soldering of BGAs 93
8.5 Design-for-Reliability (DfR) Process 98
8.6 Validation and Qualification Tests 98
8.7 Screening Procedures 99
8.7.1 Solder Joint Defects 99
8.7.2 Screening Recommendations 99

9 DEFECT AND FAILURE ANALYSIS CASE STUDIES 99
9.1 Soldermask Defined BGA Conditions 99
9.2 Over-Collapse BGA Solder Ball Conditions 99
9.3 Critical Solder Paste Conditions 100
9.4 Void Determination Through X-Ray and Microsection 100
9.5 BGA Interposer Bow and Twist 101
9.6 Solder Joint Conditions 102
9.6.1 Target Solder Condition 103
9.6.2 Excessive Oxide 103
9.6.3 Evidence of Dewetting 103
9.6.4 Mottled Condition 103
9.6.5 Cold Solder Joint 104
9.6.6 Evidence of Contamination 104
9.6.7 Deformed Solder Ball 104
9.6.8 Missing Solder Ball 105
9.6.9 Solder Bridge 105
9.6.10 Disturbed Solder 105
9.6.11 Deformed Solder Ball 106
9.6.12 Missing Solder Interface 106
9.6.13 Reduced Contact 106
9.6.14 Solder Bridge 106
9.6.15 Incomplete Solder Reflow 106
9.6.16 Disturbed Solder 107
9.6.17 Missing Solder 107

10 GLOSSARY/ACRONYMS 108

11 BIBLIOGRAPHY AND REFERENCES 109

Figures

Figure 1-1 Area Array I/O Position Comparisons 2
Figure 1-2 Area Array I/O Position Patterns 3
Figure 1-3 Application Specific Module (ASM) Ball Grid Array Format 3
Figure 1-4 Conductor Width to Pitch Relationship 5
Figure 1-5 Plastic Ball Grid Array, Chip Wire Bonded 5
Figure 1-6 Ball Grid Array, Flip Chip Bonded 6
Figure 1-7 Conductor Routing Strategy 6
Figure 1-8 MCM Type 2S-L-WB 7
Figure 3-1 BGA Warpage 11
Figure 4-1 BOC BGA Construction 14
Figure 4-2 Top of Molded BOC Type BGA 14
Figure 4-3 Cross-Section of a Plastic Ball Grid Array (PBGA) Package 19
Figure 4-4 Cross-Section of a Ceramic Ball Grid Array (CBGA) Package 19
Figure 4-5 Cross-Section of a Ceramic Column Grid Array (CCGA) Package 19
Figure 4-6 Polyimide Film Based Lead-Bond μBGA Package Substrate Furnishes Close Coupling Between Die Pad and Ball Contact 20
Figure 4-7 Comparing In-Package Circuit Routing Capability of the Single Metal Layer Tape Substrate to Two Metal Layer Tape Substrate 20
Figure 4-8 Single Package Die-Stack BGA 21

Figure 4-9 Folded Multiple-Die BGA Package 21
Figure 4-10 Ball Stack Package 21
Figure 4-11 The Standard SO-DIMM Memory Card Assembly 21
Figure 4-12 Folded and Stacked Multiple Die BGA Package 22
Figure 4-13 BGA Connector 23
Figure 4-14 Example of Missing Balls on a BGA Component 26
Figure 4-15 Example of Voids in Eutectic Solder Balls 26
Figure 4-16 Examples of Solder Ball/Land Surface Conditions 26
Figure 4-17 Establishing BGA Coplanarity Requirement 27
Figure 4-18 Ball Contact Positional Tolerance 28
Figure 5-1 Examples of Different Build-Up Constructions 29
Figure 5-2 Typical Mud Crack Appearance of Black Pad Surface 33
Figure 5-3 A Large Region of Severe Black Pad with Corrosion Spikes Protruding into Nickel Rich Layer Through Phosphorus Rich Layer Underneath Immersion Gold Surface 33
Figure 5-4 Work and Turn Panel Layout 36
Figure 5-5 Distance from Tented Land Clearance 36
Figure 5-6 Via Plug Methods 38
Figure 5-7 Solder Filled and Tented Via Blow-Out 39
Figure 6-1 BGA Alignment Marks 40
Figure 6-2 Solder Lands for BGA Components 41
Figure 6-3 Good/Bad Solder Mask Design 42
Figure 6-4 Square Array 43
Figure 6-5 Rectangular Array 43
Figure 6-6 Depopulated Array 43
Figure 6-7 Square Array With Missing Balls 43
Figure 6-8 Interspersed Array 44
Figure 6-9 Cross Section of 0.75 mm Ball with Via-in-Pad Structure (Indent to the upper left of the ball is an artifact.) 44
Figure 6-10 Cross Section of Via-in-Pad Design Showing Via Cap and Solder Ball 45
Figure 6-11 Via-In-Pad Process Descriptions 45
Figure 6-12 Example of Top Side Reflow Joints 46
Figure 6-13 Example of Wave Solder Temperature Profile of Top-Side of Mixed Component Assembly 46
Figure 6-14 Heat Pathways to BGA Solder Joint During Wave Soldering 47
Figure 6-15 Methods of Avoiding BGA Topside Solder Joint Reflow 47
Figure 6-16 An Example of a Side Contact Made With a Tweezers Type Contact 49
Figure 6-17 Pogo-Pin Type Electrical Contact Impressions on the Bottom of a Solder Ball 49
Figure 6-18 Area Array Land Pattern Testing 50
Figure 6-19 Board Panelization 53
Figure 6-20 Comb Pattern Examples 54
Figure 6-21 Heat Sink Attached to a BGA with an Adhesive 56
Figure 6-22 Heat Sink Attached to a BGA with a Clip that Hooks onto the Component Substrate 56
Figure 6-23 Heat Sink Attached to a BGA with a Clip that Hooks into a Through-Hole on the Printed Circuit Board 56
Figure 6-24 Heat Sink Attached to a BGA with a Clip that Hooks onto a Stake Soldered in the Printed Circuit Board 57
Figure 6-25 Heat Sink Attached to a BGA by Wave Soldering its Pins in a Through-Hole in the Printed Circuit Board 57
Figure 7-1 High Lead and Eutectic Solder Ball and Joint Comparison 60
Figure 7-2 Example of Reflow Temperature Profile 61
Figure 7-3 Effect of Having Solder Mask Relief Around the BGA Lands of the Board 63
Figure 7-4 Breakaway Tabs 66
Figure 7-5 Standard Scoring Parameters 66
Figure 7-6 Fundamentals of X-Ray Technology 67
Figure 7-7 X-Ray Example of Missing Solder Balls 68
Figure 7-8 X-Ray Example of Voiding in Solder Ball Contacts 68
Figure 7-9 Manual X-Ray System Image Quality 68
Figure 7-10 X-Ray Can Be Used to Detect BGA Package “Popcorning” (Pincushion Distortion) 69
Figure 7-11 Transmission Image (2D) 69
Figure 7-12 Tomosynthesis Image (3D) 69
Figure 7-13 Laminographic Cross-Section Image (3D) 70
Figure 7-14 Transmission Example 70
Figure 7-15 Oblique Viewing Board Tilt 70
Figure 7-16 Oblique Viewing Detector Tilt 70
Figure 7-17 Top Down View of FBGA Solder Joints 71
Figure 7-18 Oblique View of FBGA Solder Joints 71
Figure 7-19 Tomosynthesis 71
Figure 7-20 Scanned-Beam X-Ray Laminography 72
Figure 7-21 Scanning Acoustic Microscopy 73
Figure 7-22 Endoscope Example 73
Figure 7-23 Engineering Crack Evaluation Technique 74
Figure 7-24 A Solder Ball Cross Sectioned Through A Void in the Solder Ball 74
Figure 7-25 Cross-Section of a Crack Initiation at the Ball/Pad Interface 75
Figure 7-26 No Dye Penetration Under the Ball 75
Figure 7-27 Corner Balls have 80-100% Dye Penetration which Indicate a Crack 75
Figure 7-28 Small Voids Clustered in Mass at the Ball-to-Land Interface 78

Figure 7-29 X-Ray Image of Solder Balls with Voids at 50 kV (a) and 60 kV (b) 78
Figure 7-30 X-Ray Film Image of Voids 79
Figure 7-31 Example of Voided Area at Land and Board Interface 80
Figure 7-32 Typical Flow Diagram for Void Assessment ... 81
Figure 7-33 Void Diameter Related to Land Size 83
Figure 7-34 X-Ray Image Showing Uneven Heating 85
Figure 7-35 X-Ray Image at 45° Showing Insufficient Heating in One Corner of the BGA 85
Figure 7-36 X-Ray Image of Popcorning 85
Figure 7-37 X-Ray Image Showing Warpage in a BGA 85
Figure 7-38 BGA/Assembly Shielding Examples 86
Figure 8-1 Solder Joint Failure Due to CTE Mismatch ... 89
Figure 8-2 Grainy Appearing Solder Joint 90
Figure 8-3 Land Contamination (Black Pad or Soldermask Residue) 90
Figure 8-4 Nonsolderable Land 90
Figure 8-5 Solder Ball Pull-Away 90
Figure 8-6 Missing Solder Ball 90
Figure 8-7 Deformed Solder Joint Due to BGA Warping 91
Figure 8-8 Lifted Land (Located at Corner of BGA) 91
Figure 8-9 Insufficient Reflow Temperature Result Example 91
Figure 8-10 Solder Mask Influence 93
Figure 8-11 Reliability Test Failure Due to Very Large Void 93
Figure 8-12 Comparison of a Lead Free (SnAgCu) and SnPb BGA Reflow Soldering Profiles Void 96
Figure 8-13 Endoscope Photo of a SnAgCu BGA Solder Ball 96
Figure 8-14 Comparison of Reflow Soldering Profiles for SnPb, Backward Compatibility and Total Lead Free Board Assemblies 97
Figure 8-15 Micrograph of a Cross-Section of a BGA SnAgCu Solder Ball, Assembled onto a Board with SnPb Solder Paste using the Standard SnPb Reflows Soldering Profile. The SnAgCu Solder Ball does not Melt. Black/Grey Interconnecting Fingers are Pb Rich Grain Boundaries; Rod Shape Particles are Ag_3Sn IMCs, Grey Particles are Cu_6Sn_5 IMCs. 97
Figure 8-16 Micrograph of a Cross-Section of a BGA SnAgCu Solder Ball, Assembled onto a Board with SnPb Solder Paste using a Backward Compatibility Reflows Soldering Profile. The SnAgCu Solder Ball has Melted. 98
Figure 9-1 Soldermask Defined and Nondefined Lands 99
Figure 9-2 Soldermask Defined BGA Failures 100
Figure 9-3 Over Collapsed BGA Solder Ball 100
Figure 9-4 Extreme Collapsed Solder Ball Joints 101
Figure 9-5 Solder Paste Deposition 101
Figure 9-6 Voids and Uneven Solder Balls 101
Figure 9-7 Eggshell Void 102
Figure 9-8 BGA Interposer Warp 102
Figure 9-9 Solder Joint Opens Due to Interposer Warp 102
Figure 9-10 Uniform Solder Balls 103
Figure 9-11 Solder Balls With Excessive Oxide 103
Figure 9-12 Evidence of Dewetting 103
Figure 9-13 Overheated Surface Condition 103
Figure 9-14 Example of Cold Solder Joint 104
Figure 9-15 Incomplete Joining Due to Land Contamination 104
Figure 9-16 Solder Ball Deformation Contamination 104
Figure 9-17 Missing Solder Ball 105
Figure 9-18 Excessive Solder Bridging and Missing Ball 105
Figure 9-19 Disturbed Solder Joint 105
Figure 9-20 Deformed Solder Ball 106
Figure 9-21 Insufficient Solder and Flux for Proper Joint Formation 106
Figure 9-22 Reduced Termination Contact Area 106
Figure 9-23 Excessive Solder Bridging 106
Figure 9-24 Several Examples of Incomplete Solder Reflow 107
Figure 9-25 Disturbed Solder Joint 107
Figure 9-26 Missing Solder 107

Tables

Table 1-1 Number of Escapes Vs. Array Size on Two Layers of Circuitry 3
Table 1-2 Multichip Module Definitions 6
Table 3-1 Semiconductor Cost Predictions 11
Table 4-1 JEDEC Standard JEP95, Section 4.5 Allowable Ball Diameter Variations for FBGA ... 15
Table 4-2 Ball Diameter Sizes for PBGAs 16
Table 4-3 Future Ball Size Diameters for PBGAs 16
Table 4-4 Land Size Approximation 17
Table 4-5 Future Land Size Approximation 17
Table 4-6 Land-to-Ball Calculations for Current and Future BGA Packages (mm) 18
Table 4-7 Typical Properties of Common Dielectric Materials 25
Table 4-8 Moisture Classification Level and Floor Life 28
Table 5-1 Environmental Properties of Common Dielectric Materials 30
Table 5-2 Key Attributes for Various Board Surface Finishes 31
Table 5-3 Via Filling to Surface Finish Process Evaluation 37
Table 5-4 Via Fill Options 37
Table 6-1 Number of Conductors Between Solder Lands for 1.27 mm Pitch BGAs 41

Table 6-2 Number of Conductors Between Solder Lands for 1.0 mm Pitch BGAs 41
Table 6-3 Effects of Material Type on Conduction Materials 55
Table 6-4 Emissivity Ratings for Certain Materials 55
Table 7-1 Particle Size Comparisons 59
Table 7-2 Tolerance of Profiles, Cutouts, Notches, and Keying Slots, as Machined, mm 65
Table 7-3 Standard Scoring Parameters 66
Table 7-4 Inspection Usage Application Recommendations 67
Table 7-5 Field of View for Inspection 72
Table 7-6 Accelerated Testing for End Use Environments 77
Table 7-7 Void Classification 79
Table 7-8 Void Size Limitations 82
Table 7-9 Corrective Action Indicator 82
Table 7-10 Ball-to-Void Size Image - Comparison for Various Ball Diameters 82
Table 7-11 C=0 Sampling Plan (Sample Size for Specific Index Value*) 83
Table 7-12 Repair Process Temperature Profiles for FR-4 Material 87
Table 8-1 Typical Standoff Heights for Sn/Pb Ball 92
Table 8-2 Common Lead Free Solders, Their Melting Points, Advantages and Drawbacks 94
Table 8-3 Comparison of Lead Free Solder Alloy Compositions in the Sn-Ag-Cu Family Selection by Various Consortia 95
Table 8-4 Types of Lead Free Assemblies Possible 96

Design and Assembly Process Implementation for BGAs

1 SCOPE

This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types is also addressed. The focus on the information contained herein is on critical inspection, repair, and reliability issues associated with BGAs.

1.1 Purpose The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes. The intent is to provide useful and practical information to those who are using BGAs and those who are considering BGA implementation.

1.2 Selection Criteria (Determination of Package Style and Assembly Processes) Every electronic system consists of various parts: interfaces, electronic storage media, and the printed board assembly. Typically, the complexity of these systems is reflected in both the type of components used and their interconnecting structure. The more complex the components, as judged by the amount of input/output terminals they possess, the more complex is the interconnecting substrate.

Cost and performance drivers have resulted in increased component density, and a greater number of components attached to a single assembly, while the available mounting real estate has shrunk. In addition, the number of functions per device has increased and this is accommodated by using increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for both assemblers and bare board manufacturers. Assemblers encounter handling, coplanarity and alignment problems.

The board manufacturers must deal with land size issues, solder mask resolution and electrical test problems.

Based on industry predictions one would believe that all component packages have over 200 I/Os and are increasing in I/O count. Actually, components with the highest usage have I/O counts in the 16 to 64 I/O range. Over 50% of all components fall into this category, while only 5% of all components used have over 208 I/Os, which may be the threshold for determining the cross-over point between peripheral leaded component style packages and array type formats.

Many peripherally leaded, lower I/O count devices, such as memory and logic devices, are being converted to area array packaging formats as either BGAs or Fine Pitch BGAs.

Although the percentage of high I/O components used on an electronic assembly is small, they play a big part in driving the industry infrastructure for both bare board and assembly manufacturing. These high I/O components determine the process for bare board imaging, etching, testing and surface finishing. They determine the materials used for fabrication and drive assembly process improvements in a similar manner.

The electronics industry has evolved from using through-hole assembly technology in which the component leads went into the printed board substrate and were either soldered to the bottom side of the board or into a plated-through hole. Surface Mounting Technology (SMT) has advanced to a stage where the majority of electronic components manufactured today are only available in SMT form.

Manufacturing products with SMT in any significant volume requires automation. For low volume, a manually operated machine or a single placement machine may be sufficient. High volume SMT manufacturing requires special solder paste deposition systems, multiple and various placement machines, in-line solder reflow systems and cleaning systems.

The heart of surface mount manufacturing is the machine that places the components onto the printed board land areas prior to soldering. Unlike through-hole (TH) insertion machines, surface mount placement machines are usually capable of placing many different component types. As design densities have increased, new SMT package styles have evolved. Examples are Fine Pitch Technology (FPT), Ultra Fine Pitch Technology (UFPT), and Array Surface Mount (ASM). This latter category consists of the many families of ball or column grid arrays and the chip scale packages (CSP) and Fine Pitch BGAs (FBGA). These parts are all capable of being placed by machines provided that the equipment has the required positioning accuracy.

Increased device complexity has been a primary driving factor for SMT. In order to minimize the component package size, component lead spacing has decreased (e.g., 1.27 mm to 0.65 mm). Further increases in semiconductor integration requiring more than 196 I/Os can drive packages to even closer perimeter lead spacing, such as 0.5 mm, 0.4 mm, 0.3 mm, and 0.25 mm. However, the array package format has become the favorite for high I/O count devices. Area array component package styles have a pitch that originally was much larger than the equivalent peripherally leaded device, however that lead format is now also seeing reductions in pitch configurations.